Materials for Advanced Si CMOS

Further size reduction of complementary-metal-oxide-silicon (CMOS) devices in the Si microelectronics industry, necessary for continued adherence to Moore's law, is currently materials limited. The gate stack, composed of the SiO_2 gate dielectric and the doped polycrystalline Si gate electrode, is no longer sufficient and must be replaced by new materials. Further, starting Si wafers must be strain engineered to increase carrier mobility and subsequent device performance. NIST plays an active role in both activities.

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NIST/MSEL is poised to play important roles in the introduction of new materials to the Si microelectronics industry, so that further scaling (size reduction) may be enabled. One example is the advanced gate stack for Si CMOS. To enable further device scaling, the capacitive equivalent thickness (CET) of the gate stack must be 0.5 nm to 1.0 nm. This will not be achievable with existing SiO_2/polycrystalline Si gate stacks. Since replacements for SiO_2 have already been identified, it is now particularly important to replace the doped polycrystalline Si gate electrode with a true metal. Given the large number of possible choices of alloys for the metal gate electrode, the combinatorial approach is seen as the most effective way of identifying alloys possessing the proper work function and stability as metal gates on HfO_2.

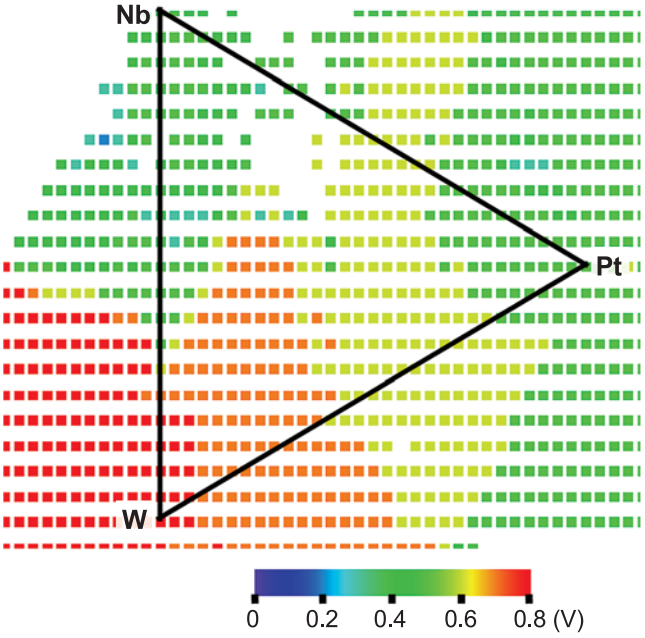

Figure 1: *Flatband voltage measurements obtained from capacitance — voltage data, for the Nb-Pt-W metal gate system.*

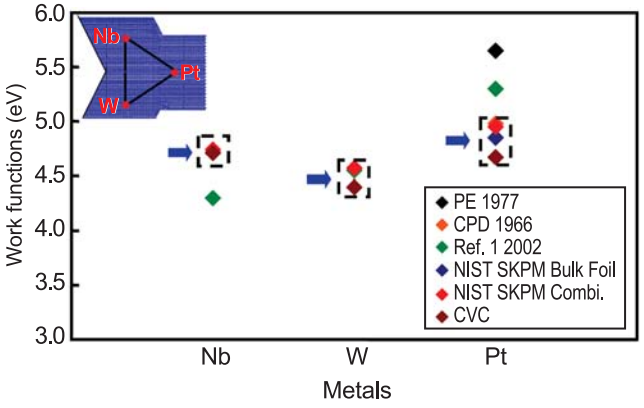

Figure 2: *Comparison of work function data determined through combinatorial experiments and other techniques.*

Figure 1 shows flatband voltage data, from which work functions may be derived, measured on hundreds of capacitors, where each small square represents a different metal gate composition in the Nb-W-Pt ternary system. Variations in flatband voltage, due to alloy composition, are readily observed. As can be seen from Figure 2, work functions determined through combinatorial experiments are in excellent agreement with those determined by other, less straightforward means.

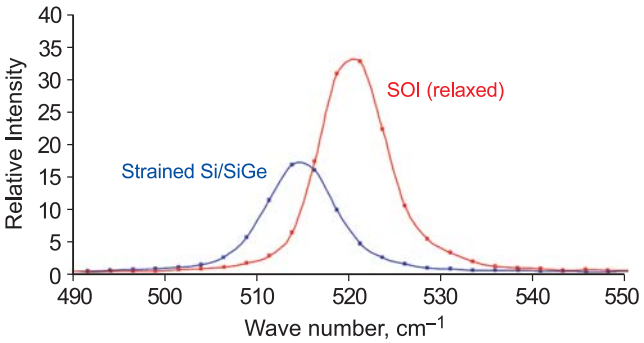

Figure 3: *Raman shift of strained Si with respect to relaxed Si.*

Another example of NIST activity in advanced Si materials is strained Si, which is increasingly being used to enhance carrier mobilities in high performance devices. Figure 3 shows the characteristic Raman shift that accompanies strain in the Si lattice. MSEL/NIST is working to calibrate the Raman shift to an absolute strain measurement (via precision lattice parameter determination) to facilitate the introduction of this technology.

Contributors and Collaborators

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